WHAT IS CLAIMED IS:

1. A memory comprising:

a plurality of memory arrays wherein each memory array has a memory array architecture similar to an apparatus architecture of an apparatus coupled to the plurality of memory arrays.

2. The memory of claim 1, wherein the apparatus architecture coupled to the plurality of memory arrays is a pipelined microprocessor architecture.

3. The memory of claim 1, wherein the apparatus architecture coupled to the plurality of memory arrays is a non-pipelined microprocessor architecture.

4. The memory of claim 2, wherein the pipelined processor supports out-of-order data processing operations and the plurality of memory arrays supports out-of-order data processing operations.

5. A memory comprising:

a plurality of memory arrays that are divided into banks, wherein said memory arrays are arranged in a pipelined architecture format and said memory arrays interoperate with a pipelined processor architecture.

6. The memory of claim 5, wherein the plurality of memory arrays that are divided into the plurality of banks support pipeline access to a plurality of data pipes that interface with the plurality of memory arrays.

7. The memory of claim 6, wherein at least one data pipe is used for a reading operation.

8. The memory of claim 6, wherein at least one data pipe is used for a writing operation.

9. The memory of claim 6, wherein there are at least eight banks in each array.

10. The memory of claim 6, wherein a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate.

11. The memory of claim 6, wherein a clock frequency and a data path width for the pipeline is determined.

12. The memory of claim 6, wherein a number of pipeline stages is related to a number of clock cycles.

13. The memory of claim 12, wherein the number of pipeline stages is the same as the number of clock cycles.

14. The memory of claim 6, wherein the pipelined memory array is divided into a horizontal arrangement.

15. The memory of claim 6, wherein the pipelined memory array is divided into a vertical arrangement.

16. The memory of claim 6, wherein a writing operation into memory is performed by pumping an address with data that is to be written into memory.

17. The memory of claim 6, wherein a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks one cycle at a time.

18. The memory of claim 6, wherein memory operations from different banks having different memory addresses are interleaved.

19. The memory of claim 6, wherein all peripheral access is accomplished from one side of a systolic memory array.

20. The memory of claim 6, wherein whenever a bank receives a read address, memory access is initiated.

21. The memory of claim 6, wherein access latency for a bank is represented by 2i + L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

22. The memory of claim 21, wherein it will take i cycles to allow data to come out of the i th bank through a read pipeline.

23. The memory of claim 21, wherein to avoid memory collisions among data, a second read access of consecutive reads delays the placement of read result on the read data pipeline by a specified idle time.

24. The memory of claim 23, wherein the specified idle time is at least one clock cycle.

25. A processing system comprising:

a die including a microprocessor;

peripheral equipment coupled to the processing system;

communication channels and paths;

a network interface; and

on-die and off-die storage media wherein said storage media is a systolic memory array.

26. The processing system of claim 25, wherein a plurality of memory arrays are divided into a plurality of banks and wherein pipeline access to a plurality of data pipes that interface with the plurality of memory arrays is enabled and supported.